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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/811,601	03/20/2001	Tetsuji Kishi	60188-045	9328

7590 07/12/2004

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EXAMINER	
NGUYEN, HAU H	
ART UNIT	PAPER NUMBER
2676	12

DATE MAILED: 07/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/811,601	KISHI ET AL.	
	Examiner	Art Unit	
	Hau H Nguyen	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-47* is/are pending in the application.

4a) Of the above claim(s) *10-31* is/are withdrawn from consideration.

5)☒ Claim(s) *1-9 and 32-40* is/are allowed.

6)☒ Claim(s) *41-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Allowable Subject Matter

1. Claims 1-9, 32-40 are allowed.

Reasons for Allowance

2. The following is an examiner's statement of reasons for allowable subject matter:

The prior art taken singly or in combination does not teach or suggest, a graphics processor among other things, comprising a graphics command storing section includes a first data storing means and second data storing means having a check address, and when an address of a graphics command being read out matches a predetermined check address, the graphics processor compares the priority of storing a graphics command to the first data storing means with the priority of the data transfer operation.

The closest prior art, Shimomura et al. (U.S. Patent No. 6,600,492) teach a receiving unit, a transferring unit, a display data generation section, and an image display section.

However, reference Shimomura et al. does not teach the above-mentioned feature.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 41-47 are rejected under 35 U.S.C. 102(e) as being anticipated by Shimomura et al. (U.S. Patent No. 6,600,492).

Referring to claims 41, 42, 45, and 46, Shimomura et al. teach a picture processing apparatus comprising, as shown in Fig. 1, a CPU 500 (external unit) for generating an instruction to be executed by the graphic processor 100 on the basis of the program. The generated instruction is then stored in the rendering-data storage area 720 of the memory unit 700 by way of the CPU bus 550, the CPU I/F circuit 310 (receiving unit) and the internal bus 110 (transferring unit). When a rendering process is started, the graphic processor 100 reads out the instruction, which has been stored in the rendering-data storage area 720 of the memory unit 700 by the CPU 500. The rendering circuit 320 (display data generation section) generates data to be displayed on the liquid-crystal display unit 20000 in accordance with the instruction and stores the data into the memory unit 700. The data stored in the memory unit 700 is then read out by the display circuit 340 (image display section) employed in the graphic processor 100 so as to be displayed on the liquid-crystal display unit 20000. In an operation to display map data as described above, the rendering circuit 320 and the display circuit 340 make accesses to the memory unit 700. At that time, the bus control circuit 200 (bus control section) arbitrates contentions for accesses between the rendering circuit 320 and the display circuit 340 (col. 5, lines 20-42). The video input circuit 330 makes an access to the memory unit 700 to write input video data into the memory unit 700 by issuing a request 333 for a right to use the internal bus 110 for making an access to the memory unit 700 to the bus control circuit 200 and waiting for an acknowledgment 334 to be output by the bus control circuit 200 in response to the request 333. (It is inherent the video input circuit to have a decoding circuit for pre-decoding graphics

command from the CPU). To put it in detail, first of all, the video input circuit 330 outputs an internal-state signal 331 indicating an estimated time, in which an internal buffer will be filled up with input video data (a processing amount estimating section), to the bus control circuit 200. If a result 332 of a judgment on a priority level output by the bus control circuit 200 to the video input circuit 330 in response to the internal-state signal 331 indicates that the priority level of the video input circuit 330 to use the internal bus 110 for making an access to the memory unit 700 is highest, the video input circuit 330 outputs the request 333 to use the internal bus 110 for making an access to the memory unit 700 immediately to the bus control circuit 200 (Fig. 4, and col. 7, lines 22-41). Thus, the bus control section changes the priority of the data transfer operation according to the data processing amount estimated by the processing amount estimating section.

In regard to claims 43, 44, and 47, Shimomura et al. teach the bus control circuit 200 compares the degrees of urgency of accesses to the memory unit 700 to be made by the CPU I/F circuit 310, the rendering circuit 320, the video input circuit 330 and the display circuit 340 by analyzing the internal-state signals 311, 321, 331 and 341 received from the CPU I/F circuit 310, the rendering circuit 320, the video input circuit 330 or the display circuit 340, respectively, in order to dynamically determines levels of priority to use the internal bus 110 for making an access to the memory unit 700 for the CPU I/F circuit 310, the rendering circuit 320, the video input circuit 330 and the display circuit 340 (different types of graphics commands) (col. 8, lines 28-54). Shimomura et al. further teach setting the priority of the devices, for example, the CPU / IF 310 or the rendering circuit 320, depending on the elapsed time generated to the bus control unit (col. 6, lines 35-67, and col. 7, lines 1-4)

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 703-305-4104. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 703-308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D. C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

H. Nguyen

07/09/2004

Kee M. Tung
Primary Examiner